IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	09/405,977	Confirmation No. 1104
Applicant	:	Ganesan et al.	
Filed	:	September 27, 1999	
Reissue App. No.	:		
For	:	METHOD AND APPARATUS FOR REDUCING STRESS ACROSS CAPACITORS USED IN INTEGRATED CIRCUITS	
Reissue of:		U.S. Patent No. 6,297,974	
Docket No.	:	42P6963	
Customer No.	:	8791	

MAIL STOP REISSUE
Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

AMENDMENT UNDER 37 CFR §1.173(b)

Sir:

In accordance with 37 C.F.R. §1.173(b), Applicant respectfully submits that the proposed amendments be incorporated into the above-identified Reissue application prepared in compliance with 37 C.F.R. §1.173(a) and enclosed herewith.

In the specification please replace the Summary of the Invention with the following.

Summary Of The Invention

A method, apparatus, and system for controlling the voltage levels across capacitors coupled between a first node and a second node of an integrated circuit so that the voltage levels across these capacitors will not exceed the breakdown voltage limitation of these capacitors. The voltage level between the first and second nodes of the integrated circuit can vary from a second voltage level to a first voltage level when the integrated circuit transitions from a second power state to a first power state, respectively. A first capacitor and a second capacitor are connected in series between the first and second nodes of the integrated circuit forming a middle node between the first and second capacitors. The voltage level of the middle node is set to a third voltage level when the integrated circuit is placed in the first power state such that the voltage level between the first and middle nodes does not exceed the breakdown voltage of the first capacitor and the voltage level between the middle and second nodes does not exceed the breakdown voltage of the second capacitor.